packaging element. By providing bus bars for power and ground voltages or shared signals, the lead frame design of the present invention increases the effective number of available electrical signal paths between the internal IC chip and a host PCB into which the IC module is installed. FIG. 2*a* shows an embodiment of the present invention to be used in a pin-type chip package. A metal lead frame **220** is stamped or etched from a thin metal sheet or strip. A central die attach platform **121** is surrounded by narrow leads **122** and bus bars **128** and **129**, all of which are rigidly maintained by a skirt **123**. An IC chip **110** mounted on platform **121** includes multiple I/O pads **111** for power and signal connections to IC chip **110**. Signal I/O pads are wire bonded to leads **122** by wires **114**. All power I/O pads are wire bonded to bus bar **128**, and all ground I/O pads are connected to bus bar **129**. Subsequent encapsulation by a casing **130** and formation of pin-type IC-PCB interconnections **140** as shown in FIG. 2*b* is performed as in a conventional IC module. Because bus bars **128** and **129** provide a common attachment area for multiple power and ground I/O pads, the total number of signal I/O pads on IC chip **110**, and therefore chip pinout, is increased over the conventional design shown in FIG. 1*a*.

FIG. 2*c* depicts an embodiment of the present invention incorporated into a lead frame ball grid array (BGA) package. Metal lead frame **220** is stamped or etched from a thin metal sheet or strip. Central die attach platform **121** is surrounded by narrow leads **122** and bus bars **127**, all of which are rigidly maintained by skirt **123**. A circular attachment pad **126** is located at the end of each lead **122**. IC chip **110** includes multiple I/O pads **111** and is mounted on the top surface of platform **121**. Signal I/O pads are wire bonded to circular attachment pads **126** by wires **114**. All power I/O pads are wire bonded to bus bars **127**, while all ground I/O pads are connected to platform **121**. Installation of protective casing **160** and removal of skirt **123** is performed in the same manner as in conventional lead frame BGA packages, as indicated in FIG. 2*d*. Mask **170** provides vias through which solder balls **150** are mounted on the bottom surface of lead frame **220**. However, because attachment pads **126** define circular areas for the application of solder balls **150**, mask **170** can simply mask each lead up to the edge of the attach pad **126**, and is not required to provide difficult-to-produce circular vias. Proper location of attachment pads **126** can even completely eliminate the need for masking leads **122**. Circular attachment pads **126** provide an inherent solder flow boundary, ensuring consistent post-installation solder ball profiles. In addition, by connecting the solder balls **150** mounted on the bottom surface of platform **121** to the ground potential of the host PCB, platform **121** can be used as a ground bus bar for IC chip **110**. Therefore, because bus bars **127** and platform **121** provide a common attachment area for multiple power and ground I/O pads, respectively, the total number of signal I/O pads on IC chip **110**, and therefore chip pinout, is once again increased over the conventional design shown in FIG. 1*c*.

In this manner, the present invention allows greater flexibility in IC chip design by enabling the use of larger numbers of bonding pads for signal communications. The lead frame design of the present invention is compatible with conventional manufacturing procedures and processes. It should be noted that while particular embodiments of the present invention have been shown and described, it will be apparent to those skilled in the art that many modifications and variations thereto are possible, all of which fall within the true spirit and scope of the invention. For example, the bus bar design can be incorporated into any IC packaging

module using a lead frame component, including dual in-line packages (DIP), quad flat pacs, plastic leaded chip carriers (PLCC), and lead frame ball grid array packages (BGA). In addition, the lead frame configuration is not intended to be limited to construction of lead frame **220** shown in FIGS. 2*a*–2*d*. The size, orientation, and location of bus bars can be varied to provide optimum performance and convenience for a specific situation. Also, while the described embodiments include two bus bars, there is no restriction on the number of bus bars that can be incorporated into a particular implementation, and bus bars can be used to distribute data as well as power signals. Finally, a bus bar can even be used as a PCB interconnect to assist in signal distribution on the host PCB.

We claim:

1. An integrated circuit package comprising,

(a) a lead frame comprising:

a die attach platform; and

a plurality of elongated leads which are electrically isolated from said die attach platform, each of said elongated leads including a circular portion formed as an attachment pad; and

(b) a substrate, having first and second surfaces on opposite sides of said substrate, for providing rigid support to said lead frame, said substrate contacting said lead frame on said first surface and having vias of non-circular cross sections to allow electrical connections between said first and second surfaces.

2. The package of claim **1**, further comprising a first bus bar which is electrically isolated from said die attach platform and said plurality of elongated leads.

3. The package of claim **2** wherein:

said lead frame further comprises a second bus bar which is electrically isolated from said die attach platform, said plurality of elongated leads, and said first bus bar;

said die attach pad is positioned between said first and second bus bars; and

said plurality of elongated leads extend radially away from said first and second bus bars and said die attach platform.

4. The package of claim **3** further comprising an integrated circuit chip mounted on said die attach platform, said integrated circuit chip having a plurality of power I/O pads, a plurality of ground I/O pads, and a plurality of signal I/O pads, wherein:

each of said plurality of signal I/O pads is electrically connected with a selected one of said plurality of leads;

said plurality of power I/O pads are electrically connected to said first bus bar; and

said plurality of ground I/O pads are electrically connected to said second bus bar.

5. The package of claim **3** further comprising an integrated circuit chip mounted on said die attach platform, said integrated circuit chip having a plurality of power I/O pads, a plurality of ground I/O pads, and a plurality of signal I/O pads, wherein:

each of said plurality of signal I/O pads is electrically connected with a selected one of said plurality of leads;

said plurality of power I/O pads are electrically connected to said first bus bar or said second bus bar; and

said plurality of ground I/O pads are electrically connected to said die attach platform.

6. The package of claim **1**, wherein an integrated circuit chip is attached on said die attach platform, said package further comprising:

a mask layer formed on said second surface, said mask layer defining a plurality of openings exposing said vias; and

a plurality of solder balls, each of said plurality of solder balls being electrically connected to one of said attachment pads by solder through one of said openings and one of said vias.

7. The package of claim **6** wherein said mask layer comprises a solder mask.

8. The package of claim **7** wherein said mask layer comprises a plated layer, the material of said plating layer being resistant to solder flow.

9. The package of claim **4** wherein:

said first bus bar is electrically connected to one of said plurality of leads that is designated to be electrically connected to the external power supply of said integrated circuit chip;

said second bus bar is electrically connected to the one of said plurality of leads that is designated to be electrically connected to ground potential; and

said lead frame and said integrated circuit chip are encapsulated in a protective casing.

10. In an integrated circuit (IC) package for accommodating an IC chip, wherein said IC chip includes a plurality of I/O pads for signal communications and a portion of said

plurality of said I/O pads require a common signal, a method comprising the steps of:

providing a lead frame having (a) a die attach platform; and (b) a plurality of leads, each lead having a circular portion formed as an attachment pad;

providing a substrate having first and second surfaces on opposite sides of said substrate to provide rigid support to said lead frame, said substrate having vias of non-circular cross sections to allow electrical connections between said first and second surfaces;

attaching said lead frame to said first surface of said substrate;

attaching said IC chip to said die attach platform;

electrically connecting said [said] I/O pads to said bus bar and said attachment pads;

providing a solder mask on said second surface of said substrate, said solder masks having openings corresponding to said vias; and

attaching solder balls to said solder mask and providing a flow of solder into said opening and said vias, said solder reaching said attachment pads so that an electrical connection is made between each solder ball and an I/O pad of said I/C chip.